IN THE CLAIMS

1. (Original) A semiconductor device, comprising:

first and second semiconductor substrates having respective opposite surfaces disposed in opposition to each other;

a first semiconductor element formed in said opposite surface of said first semiconductor substrate and comprised of a first semiconductor circuit and a first electrode;

a second semiconductor element formed in said opposite surface of said second semiconductor substrate and comprised of a second semiconductor circuit and a second electrode;

a first wiring conductor layer formed of an electrically conductive material and interposed between said first and second electrodes; and

a through electrode extending through said first semiconductor substrate and connected to said first and second electrodes through the medium of said first wiring conductor layer,

wherein said second semiconductor substrate is disposed above said first semiconductor substrate and disposed on a lateral side of said through electrode, being distanced therefrom;

wherein lateral surface of said through electrode projecting from said first semiconductor substrate and lateral surface of said second semiconductor element are coated with an insulation material layer;

wherein said through electrode has one end portion exposed from a back surface of said first semiconductor substrate to serve as a first external terminal; and

wherein said through electrode has the other end portion positioned at a same height as a back surface of said second semiconductor substrate and exposed from said insulation material layer to serve as a second external terminal.

2. (Original) The semiconductor device according to claim 1,

wherein said semiconductor device further includes a first additional external terminal exposed from a back surface of said first semiconductor substrate in a region in which said second semiconductor substrate is mounted.

3. (Original) The semiconductor device according to claim 1,

wherein the back surface of said second semiconductor substrate is coated with an insulation material.

4. (Original) The semiconductor device according to claim 3,

wherein said semiconductor device includes a second wiring conductor layer of an electrically conductive material deposited on a surface of the insulation material of said first and second semiconductor substrates and an exposed surface of said second external terminal, and

wherein said second wiring conductor layer is connected to said through electrode at a portion thereof which is exposed as said second external terminal.

5. (Original) The semiconductor device according to claim 1,

wherein an element interconnecting protrusion electrode is provided between said first electrode and said second electrode, and

wherein said first semiconductor element and said second semiconductor element are interconnected through the medium of said element interconnecting protrusion electrode.

6. (Original) The semiconductor device according to claim 1,

wherein a device connecting protrusion electrode projecting from the exposed surface of said through electrode is provided in association with at least one of said first external terminal and said second external terminal, and

wherein said device interconnecting protrusion electrode is employed as an external terminal.

7. (Original) The semiconductor device according to claim 1,

wherein an SOI (silicon oxide insulation) substrate is employed for forming said first semiconductor substrate, and

wherein an SOI insulation film is exposed as the back surface of said first semiconductor substrate.

8. (Original) The semiconductor device according to claim 7,

wherein a third wiring conductor layer is deposited on said SOI insulation film of said first semiconductor substrate, said third wiring conductor layer being connected to said first external terminal.

9. (Original) The semiconductor device according to claim 1,

wherein an SOI (silicon oxide insulation) substrate is employed as said second semiconductor substrate, and

wherein said SOI substrate includes an exposed SOI insulation film formed in the back surface of said second semiconductor substrate.

10. (Original) The semiconductor device according to claim 1,

wherein a plurality of the semiconductor devices set forth in claim 1 is interconnected through the medium of said first external terminal and/or said second external terminal.

11. (Original) The semiconductor device according to claim 10,

wherein said semiconductor device further comprises a third semiconductor substrate mounted on said second semiconductor substrate; and

a third semiconductor element formed in said third semiconductor substrate and comprised of a third semiconductor circuit and a third electrode,

wherein said third electrode is connected to said second external terminal, and

wherein lateral surface of said third semiconductor element and a surface of said third semiconductor substrate in which said third semiconductor circuit is formed are coated with an insulating material.

12. (Original) The semiconductor device according to claim 1,

wherein said through electrodes and said first semiconductor circuits are formed in pairs, respectively, in said first semiconductor substrate,

wherein said second semiconductor elements are disposed with said second electrodes being connected to the first electrodes of said plurality of first semiconductor circuit, respectively; and

wherein the surfaces of said first and second semiconductor substrate in which said first and second semiconductor circuits are formed, respectively, lateral surfaces of said second semiconductor substrates, and lateral surfaces of said through electrodes, respectively, are coated with an insulation material to thereby implement an integral planar array structure on a single board constituted by said first semiconductor substrate.

13. (Original) The semiconductor device according to claim 12,

wherein a plurality of semiconductor elements are stacked in at least one of said semiconductor devices connected to the first electrodes of said plurality of first semiconductor circuits.

Claims 14-20 (Cancelled)